# Laboratory Report # 3

**Name:** Machacon, Zach Riane  **Date Completed:** September 22, 2023

**Laboratory Exercise Title:** Structural Modeling of Combinational Circuits

***Target Course Outcomes:***

**CO1:** Create descriptions of digital hardware components such as in combinational and sequential circuits using synthesizable Verilog HDL constructs.

**CO2:** Verify the functionality of HDL-based components through design verification tools.

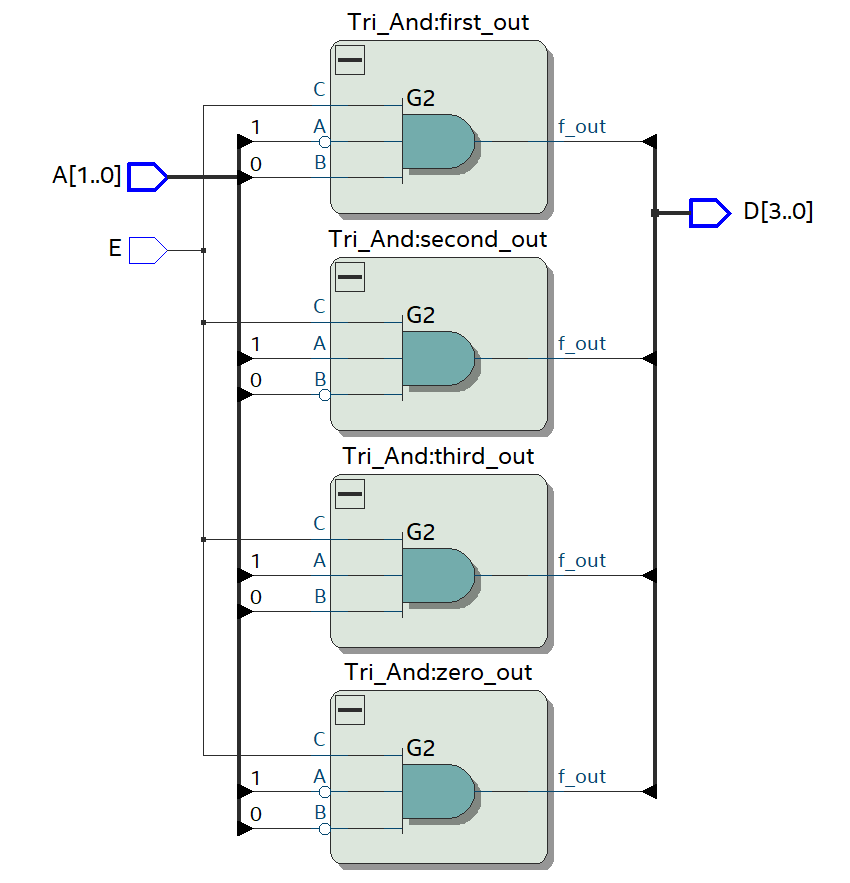
**Exercise 3A:**

**Solution:**

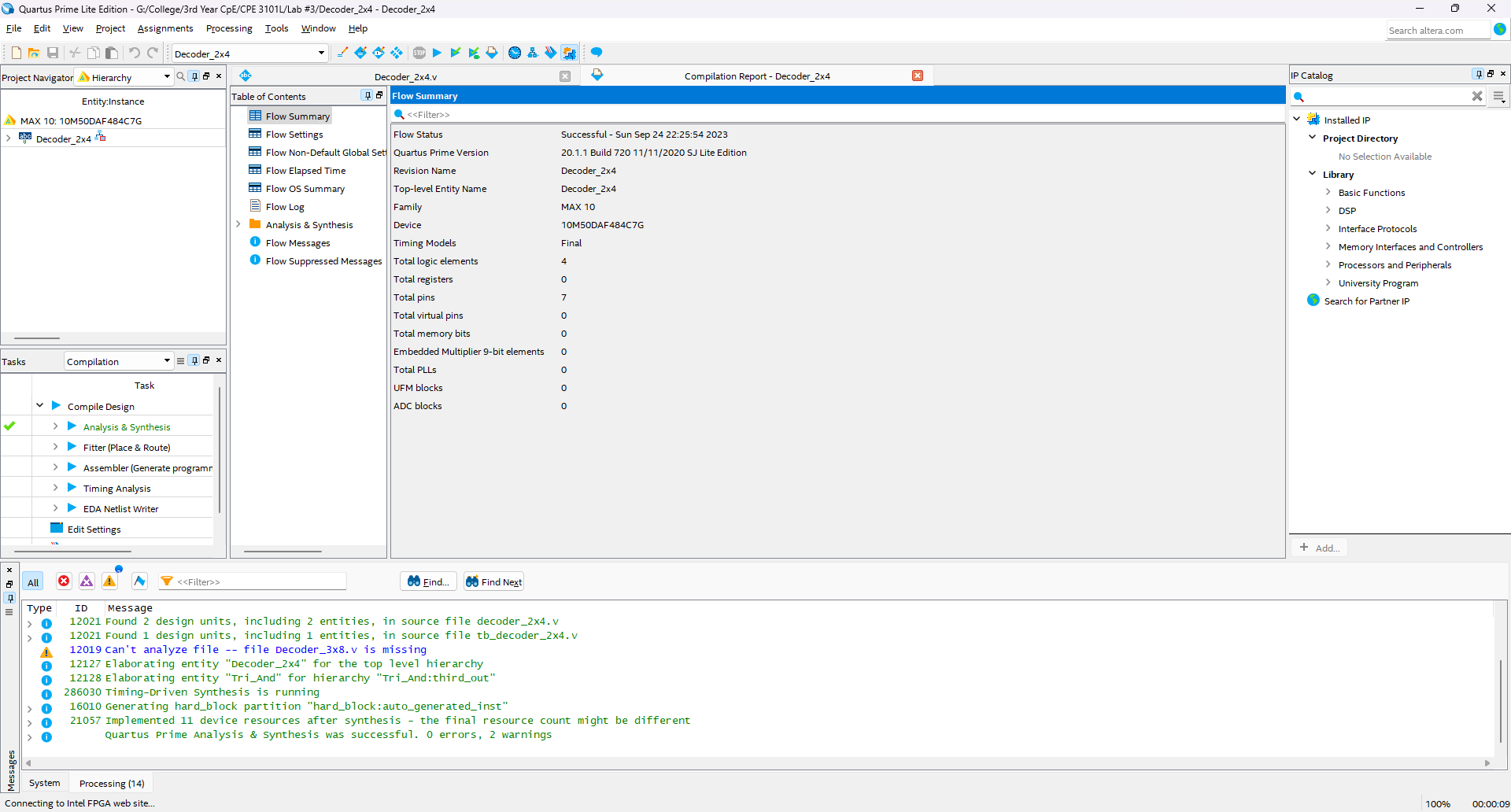
Truth Table for 2x4 Decoder

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **E** | **A1** | **A0** | **D3** | **D2** | **D1** | **D0** |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 |

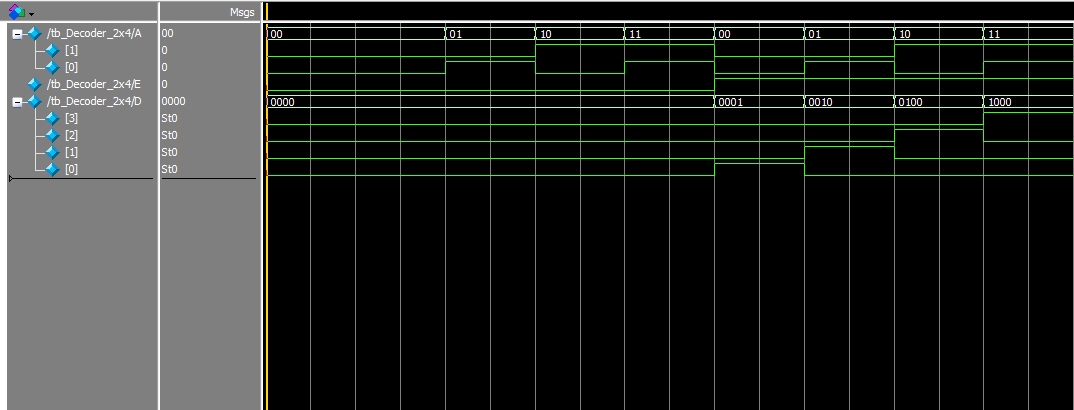
**Boolean Expressions:**

****

**Figure 1: Logic Diagram with Labels of Decoder\_2x4**



**Figure 2: Successful Design Synthesis of Decoder\_2x4**



E A[1] A[0]

1 1 1

D[3] D[2] D[1] D[0]

1 0 0 0

E A[1] A[0]

1 1 0

D[3] D[2] D[1] D[0]

0 1 0 0

E A[1] A[0]

1 0 1

D[3] D[2] D[1] D[0]

0 0 1 0

E A[1] A[0]

1 0 0

D[3] D[2] D[1] D[0]

0 0 0 1

E A[1] A[0]

0 1 1

D[3] D[2] D[1] D[0]

0 0 0 0

E A[1] A[0]

0 1 0

D[3] D[2] D[1] D[0]

0 0 0 0

E A[1] A[0]

0 0 1

D[3] D[2] D[1] D[0]

0 0 0 0

E A[1] A[0]

0 0 0

D[3] D[2] D[1] D[0]

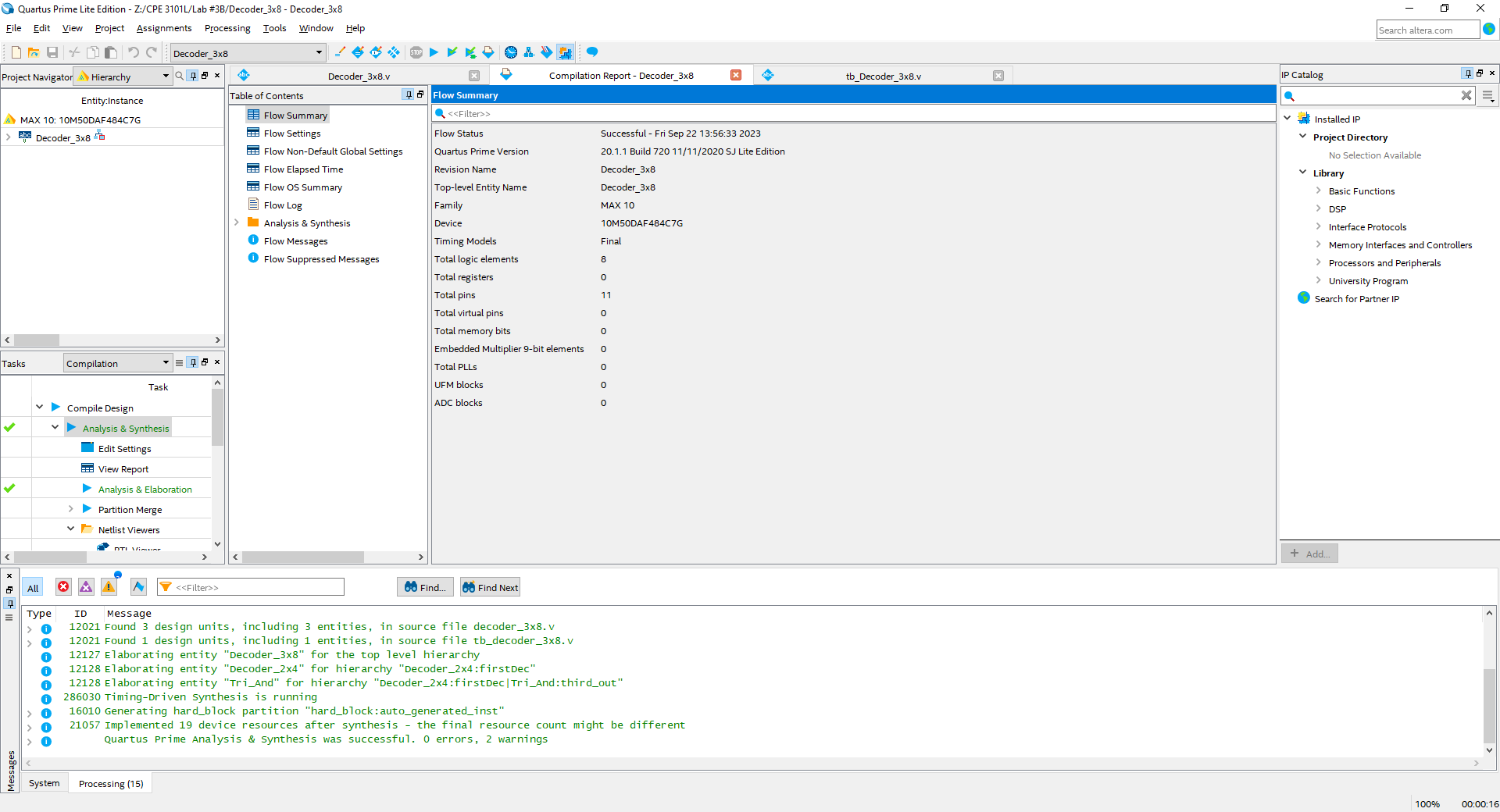
0 0 0 0

**Figure 3: Successful Simulation Results of Decoder\_2x4**

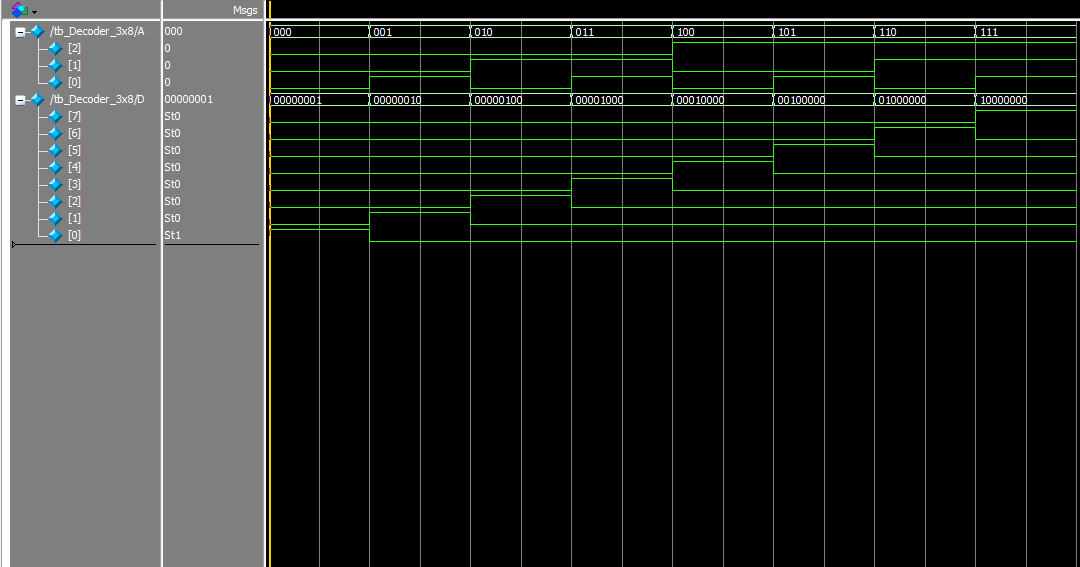
A screenshot of a computer program

Description automatically generated

**Figure 4: Internal Block Diagram of Decoder\_3x8**



**Figure 5: Successful Design Synthesis of Decoder\_3x8**



A[2] A[1] A[0]

1 1 1

D[7] D[6] D[5] D[4]

1 0 0 0

D[3] D[2] D[1] D[0]

0 0 0 0

A[2] A[1] A[0]

1 1 0

D[7] D[6] D[5] D[4]

0 1 0 0

D[3] D[2] D[1] D[0]

0 0 0 0

A[2] A[1] A[0]

1 0 1

D[7] D[6] D[5] D[4]

0 0 1 0

D[3] D[2] D[1] D[0]

0 0 0 0

A[2] A[1] A[0]

1 0 0

D[7] D[6] D[5] D[4]

0 0 0 1

D[3] D[2] D[1] D[0]

0 0 0 0

A[2] A[1] A[0]

0 1 1

D[7] D[6] D[5] D[4]

0 0 0 0

D[3] D[2] D[1] D[0]

1 0 0 0

A[2] A[1] A[0]

0 1 0

D[7] D[6] D[5] D[4]

0 0 0 0

D[3] D[2] D[1] D[0]

0 1 0 0

A[2] A[1] A[0]

0 0 1

D[7] D[6] D[5] D[4]

0 0 0 0

D[3] D[2] D[1] D[0]

0 0 1 0

A[2] A[1] A[0]

0 0 0

D[7] D[6] D[5] D[4]

0 0 0 0

D[3] D[2] D[1] D[0]

0 0 0 1

**Figure 6: Successful Simulation Results of Decoder\_3x8**